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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,731	09/18/2003	Shunpei Yamazaki	0553-0187.01	5614
7590 06/14/2005				
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		EXAMINER		
		COLON, GERMAN		
		ART UNIT		PAPER NUMBER
		2879		

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/664,731

Applicant(s)

YAMAZAKI ET AL. 

Examiner

German Colón

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 60, 62-65, 67-71 and 73-78 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 62-65, 67-71 and 73-78 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/587,369.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/3/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 25, 2005 has been entered.

Response to Amendment

2. The Amendment, filed on April 25, 2005, has been entered and acknowledged by the Examiner.
3. Cancellation of claim 72 has been entered.
4. Addition of claims 77-78 has been entered.

Specification

5. The disclosure is objected to because of the following informalities:

On Page 16, 4th paragraph, lines 1 and 3, references to pixel electrode **46** and passivation film **45** are made. However, line 5 refers to a pixel electrode **45**.

On Page 32, 2nd paragraph, line 1, a reference to passivation film **348** is made; while the 4th paragraph, line 1 refers to a pixel electrode **349**. However, Page 33, line 2, mentions a pixel electrode **348**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 60, 62-65, 67, 69, 71 and 73-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US 6,239,470) in view of Yudasaka (US 6,359,606).

Regarding claim 60, Yamazaki discloses a method of manufacturing a display device comprising the steps of:

forming a plurality of TFTs over a substrate **101**;

forming an insulating film **114** comprising a resin over the plurality of TFTs;

forming a passivation film **116** over the insulating film (see Col. 4, lines 26-27); and

forming a first electrode **117** over and in contact with the passivation film, wherein said first electrode is electrically connected to one of said TFTs through a contact hole through said passivation film and insulating film (see Fig. 2B). Yamazaki teaches this structure to be used for driving an EL display (see at least Col. 1, lines 10-14) but is silent regarding the components of the EL display.

However, in the same field of endeavor, Yudasaka discloses an organic EL element comprising a first electrode, a light emitting layer formed on the first electrode by an ink jet method (see Col. 9, lines 5-7) and a second electrode formed on the light emitting layer, wherein the EL element is driven by an active matrix device comprising a plurality of TFTs. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

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provide an EL layer and a second electrode to the device of Yamazaki since Yamazaki teaches the desirability of using the device for driving an EL display. Further, Yudasaka teaches to be conventional and well known in the art to drive an EL display with a device comprising a plurality of TFTs. Moreover, EL displays require a light-emitting layer sandwiched between two electrodes.

Regarding claims 62 and 63, Yamazaki discloses the passivation film 116 comprising SiN (see Col. 4, lines 26-27).

Regarding claim 64, Yamazaki-Yudasaka discloses the EL material comprising an organic light-emitting layer (see '606, at least Col. 9, lines 3-6).

Referring to claim 65, Yamazaki-Yudasaka discloses the claimed invention except for the limitation of "forming a second passivation film over the EL element".

However, Yudasaka discloses an EL display having a passivation film made of silicon nitride over an electroluminescent element with the purpose of inhibiting the deterioration of the device by protecting the EL element from oxygen and moisture (see Col. 10, lines 65-67, in view of Col. 1, lines 50-53 and Col. 6, lines 55-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a passivation film over the electroluminescent element in order to inhibit the deterioration of the device by protecting the EL element from oxygen and moisture.

Referring to claim 67, Yamazaki-Yudasaka discloses each of the first and second passivation films comprising SiN (see '470, Col. 4, lines 26-27; and '606, Col. 10, lines 65-67).

Referring to claim 69, Yamazaki discloses an insulating film comprising SiO₂ between the substrate and the plurality of TFT. However, the reference discloses the suitability of SiN as

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an insulating layer (see Col. 3, lines 63-65). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiN instead of SiO₂, since Yamazaki teaches the suitability of the former to replace SiO₂ as an insulating layer.

In regards to claim 71, Yamazaki-Yudasaka discloses a method of manufacturing a display device comprising the steps of (see Fig. 2C of '470):

forming a plurality of TFTs over a substrate **101**;

forming a leveling film **114** comprising a resin over the plurality of TFTs;

forming a passivation film **116** over the insulating film;

forming an EL element over the passivation film, said EL element comprising a first electrode in contact with the passivation film, a second electrode and a light emitting layer interposed therebetween. Same reasons for combining stated in claim 60 apply.

In regards to claim 73, Yamazaki discloses the passivation film comprising SiN (see Col. 4, lines 26-27).

In regards to claim 74, Yamazaki-Yudasaka discloses the EL material comprising an organic light emitting layer (see '606, at least Col. 9, lines 3-6).

Regarding claims 75 and 76, Yamazaki-Yudasaka discloses a device and a method of manufacturing said device, comprising (see Fig. 2C of '470):

forming a TFT over a substrate **101**;

forming a first insulating layer **112** comprising SiN or SiO_xN_y over the TFT;

forming a leveling film **114** comprising a resin over the first insulating film;

forming a second insulating film **116** comprising SiN;

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forming a light emitting element (see US `606) over the second insulating film, said light emitting element comprising a first electrode in contact with the second insulating film, a second electrode and an organic EL material interposed therebetween; and

forming a third insulating layer comprising SiN (see 60 in `606). Same reasons for combining stated in claims 60 and 65 apply.

8. Claims 68 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki-Yudasaka as applied to claim 65 above, and further in view of Kikukawa et al. (US 6,329,036).

Regarding claim 68, Yamazaki-Yudasaka discloses the passivation layers comprising silicon nitride, but is silent regarding the limitation of said layers comprising Si, Al, N, O and a rare earth element.

However, Kikukawa discloses a semiconductor device comprising an insulating film, and teaches a silicon nitride film and a rare earth-containing SiAlON film as art recognized equivalent materials. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rare earth-containing SiAlON film, as disclosed by Kikukawa, instead of a silicon nitride film, as disclosed by Yamazaki-Yudasaka, since Kikukawa teaches both films to useful insulating materials and art recognized equivalents (see Col. 8, lines 9-13). Further, it has been held to be within the general skill of an artisan to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

Regarding claim 70, claim 70 is rejected over the reasons stated in the rejection of claim 68.

9. Claims 77 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki-Yudasaka as applied to claim 76 above, and further in view of Utsugi (US 5,747,930).

Yamazaki-Yudasaka discloses the claimed invention except for the limitation of providing a pixel electrode between the first electrode and the second insulating layer.

However, in the same field of endeavor, Utsugi discloses an organic EL device (see Fig. 3) comprising a plurality of TFTs, wherein a pixel electrode 57 is formed between a first electrode 55 and an insulating layer 53b with the purpose of acting as an electrode protection layer which improves driving stability and physical stability, achieving low power consumption (see Col. 3, lines 17-20). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a pixel electrode between the first electrode and the second insulating layer of Yamazaki-Yudasaka, in order to obtain an electrode protection layer which improves driving stability and physical stability, achieving low power consumption.

10. Claims 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki-Yudasaka as applied to claim 76 above, and further in view of Tang et al. (US 5,684,365).

Yamazaki-Yudasaka discloses the claimed invention except for the limitation of forming a storage capacitor.

However, in the same field of endeavor, Tang discloses an organic EL device (see Fig. 3) comprising a plurality of TFTs, wherein a storage capacitor is formed with the purpose of enabling the excitation power to an addressed EL element to stay on once it is selected; thus the circuit provides a memory that allows the EL element to operate at a duty cycle close to 100%, regardless of the time allotted for addressing (see at least col. 6, lines 16-20). Hence, it would

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have been obvious to one of ordinary skill in the art at the time the invention was made to provide a storage capacitor to the device of Yamazaki-Yudasaka, in order to enable the excitation power to an addressed EL element to stain on once it is selected; thus the circuit provides a memory that allows the EL element to operate at a duty cycle close to 100%, regardless of the time allotted for addressing.

Response to Arguments

11. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

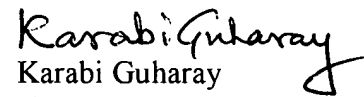
Any inquiry concerning this communication or earlier communications from the examiner should be directed to German Colón whose telephone number is 571-272-2451. The examiner can normally be reached on Monday thru Thursday, from 8:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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